IN THE SPECIFICATION:

Please amend Page 3, lines 19 through Page 4, line 8 as follows:

In 1997, researchers at HSG-IMIT reported a 10μm-thick, x-axis gyroscope using epitaxially-grown polysilicon as a structural material as discussed in W. Geiger, B. Folkmer, J. Merz, H. Sandmaier, and W. Lang, "A new silicon rate gyroscope,", in *Proc. IEEE Workshop on Microelectromech. Syst. (MEMS'98)*, Heidelberg, Germany, Feb. 1998, pp. 615-620. The device showed a 0.096 °/sec resolution with a 50 Hz bandwidth. Researchers at Samsung also reported a gyroscope using the SOI (Silicon on Insulator) process which showed a resolution of 0.015 °/sec with a 25 Hz bandwidth as discussed in K. Y. Park, H. S. Jeong, S. An, S. H. Shin, and C. W. Lee, "Lateral gyroscope suspended by two gimbals through high aspect ratio ICP etching," in *Tech. Dig. 10th Int. Conf. Solid-State Sensors and Actuators (Transducers '99)*, Sendai, Japan, June 1999, pp. 972-975 and an other gyroscope using an anodically bonded wafer which showed a resolution of 0.01 °/sec at a 5 Hz angular-rate input as discussed in S. S. Baek, Y. S. Oh, B. J. Ha, S. D. An, B. H. an, H. Song, and C. M. Song, "A symmetrical z-axis gyroscope with a high aspect ratio using simple and new process," in *Proc. IEEE Workshop on Microelectromech. Syst. (MEMS'99)*, Orlando, FL, Jan. 1999, pp. 612-617.

Please amend Page 8, lines 1 through 13 as follows:

FIG 4. is a structure formed by yet another conventional isolation method, the trench oxide isolation method, described in the following references: U.S. Patent No. 5,930,595; U. Sridhar et al., "Trench Oxide Isolated Single Crystal Silicon Micromachined Accelerometer," *IEEE IEDM*, San Francisco CA, Dec. 6-9, 1998. pp. 475-478; and S. Lee, S. Park, D. Cho and Y. Oh "Surface/Bulk

Micromachining (SBM) Process and Deep Trench Oxide Isolation Method for MEMS", *IEEE IEDM*, Washington, D.C., December 5-8, 1999. pp. 701-704. This trench isolation method includes forming U-shaped trenches ~~14~~ 104 on a silicon substrate ~~16~~ 102, forming thermal oxide layers ~~18~~ 106 and depositing oxide ~~layers 20~~ 108 on all sides of the structure where the trenches are formed. (An unfilled tubular volume 109 may be defined towards the bottom of the trench). The oxide films ~~18, 20~~ 106, 108 filling the trenches attach the electrode structures ~~22, 24~~ 112 to the silicon substrate ~~16~~ 102 through the respective sidewalls so that the oxide films support the electrodes and tethered structures. The oxide films electrically isolate the electrodes from each other and from the substrate. An area of substrate material 110 is enclosed within each trench 104. These areas 110 are referred to as "islands". These islands 110 are surrounded on three sides and on the bottom by the thermal oxide 106 and trench fill oxide 108 defined in the trenches 104. One side 111 of the islands is not covered by the insulating oxides 106, 108 of the trenches. The sensor beam 112 is connected to the islands at this uncovered side 111. This connection is the anchor portion of the beam.

Please amend Page 14, lines 18 through Page 15, line 3 as follows:

Fig. 7 shows a fabrication example of oxide/polysilicon/metal triple layer isolation method, which is a cross section of a gyroscope fabricated in this embodiment. The thickness of the oxide, polysilicon, and metal films measured at the top side of wafer are 0.12μm, 0.18μm, and 0.35μm, respectively. The trench depth is 40μm, and the opening width is 8μm. Fig. 7a shows the upper part of the trench. All the oxide, polysilicon and Al films are clearly visible at the top. On the sidewall, however, Al film is not deposited beyond several μm from the top. In Fig. 7b, which shows the lower part of the trench, the oxide and polysilicon films are uniformly deposited on both the sidewall

and the bottom surface facing the substrate. No Al film is visible on any of the surfaces in this lower part. This allows utilizing the entire sidewall to maximize capacitance.

Please amend Page 17, lines 3 through 8 as follows:

An example of micro-gyroscope is shown in Fig. 9. The driving and sensing mode resonant frequencies are designed to be 4.58 kHz and 5.76 kHz, respectively. In the composited beam analysis using (1), the undercut of 2500Å, the oxide thickness of 1200Å, and the polysilicon thickness of 1800Å are considered. The resonant frequency of sensing mode is designed to be about 1200 Hz higher than that of driving mode, since the resonant frequency of sensing mode can be easily lowered with electrostatic tuning.

Please amend Page 17, line 25 through Page 19, line 21 as follows:

The spring constant of the concatenated spring is calculated using a commercial software, ANSYS. Fig. 11 summarizes the simulation results. In the simulation of concatenated spring, the unit spring of Fig. 10 is assumed. The spring constant of the concatenated spring is slightly larger than that of the simple spring for the same spring length and width. The spring width of 4μm, thickness of 40μm, and concatenation at every 72μm are assumed for both cases.

In this embodiment, a single-crystalline-silicon micro-gyroscope is fabricated in a single wafer using the SBM process and the oxide/polysilicon/metal triple layer isolation method. The structural thickness of fabricated micro-gyroscope is 40μm, and the sacrificial gap is 50μm. The chip size is 2.2mm x 3mm. Only a single mask is required to fabricate the micro-gyroscope. The large sacrificial gap of 50μm is beneficial in terms of reducing air damping, and thus, increasing the Q-factor.

The fabrication process starts with an *n*-type, (111)-oriented silicon wafer with a resistivity of 10 mΩ. A plasma-enhanced chemical vapor deposition (PECVD) oxide layer is deposited and patterned. The deposited oxide layer is used as a hard mask for deep silicon etching. Next, a vertical, deep silicon RIE is performed to a depth of 40μm to define the structural patterns. The first oxide layer should be thick enough to withstand the vertical silicon RIE steps for structure patterning and sacrificial-gap definition, as well as the final aqueous alkaline etching for releasing the structures. In the standard Bosch process, the etch depth is highly dependent on the opening width. Thus, it is important to design all opening width to be about the same in order to have a uniform etch depth. In our design, the minimum opening width is 2μm and the maximum is 15μm. The maximum opening width is the required dimension for resonating the structure. The final structure thickness becomes the etch depth at the smaller openings.

After the structure patterning step, a 1200Å-thick thermal oxide film is grown. The film is used to protect the structure sidewalls in alkaline etching. This oxide film is then anisotropically etched using RIE to expose bare silicon at the bottom of the etched patterns. This step should not etch the oxide on sidewalls and should not expose bare silicon at the top. Then, the silicon wafer is vertically etched again using deep silicon RIE. The etch depth at the larger opening measured from the first etch depth at the smaller opening is 50μm. This results in a sacrificial gap of 50μm. The wafer is then dipped into a 20%, 90°C tetramethyl ammonium hydroxides (TMAH) solution for 15 minutes, to perform the release etch. In this step, the lower parts of the sidewalls without the oxide passivation will be etched in the lateral direction. The etch rate in <110> directions is about 95μm/hr in this etch condition. After the release etch step, all sidewall passivation oxide and top oxide films are removed in an HF solution.

After that, the oxide/polysilicon/metal triple layer isolation process is performed. For isolation, a 1200Å-thick thermal oxide film is grown. Next an LPCVD polysilicon film is deposited to a thickness of 1800Å. Note that the undercut in our deep etch process is about 2500Å. The deposition temperature is 585°C, and the as-deposited residual stress is 30 Mpa in a tensile state. For doping of polysilicon films, the predeposition of phosphorus-containing oxide is performed at the atmospheric pressure and 900°C for 10 minutes, with 2000 sccm of N_2, 400 sccm of $POCl_3$-containing N_2, and 200 sccm of O_2. Then a 3500Å-thick, 1% silicon-containing Al film is sputtered at the top. This Al film is used for the electrodes, and also serves as the hard mask for the ensuing polysilicon anisotropic etch to remove the lines and areas of polysilicon at the bottom for electrical isolation.

Please amend Page 20, lines 1 through 8 as follows:

The performance of the fabricated micro-gyroscope is experimentally evaluated. Fig. 14 shows the measurement scheme. In the testing, the feedback control for generating self-oscillation of driving mode is not used. However, the combs for sensing driving mode can monitor the displacement induced by the driving-mode vibration. To vibrate the gyroscope, a 2.5 volt peak-to-peak sinusoidal voltage 142 with a 0.8 volt offset is applied to the driving-comb electrode 1 141. The driving-comb electrode 2 143 is oppositely placed to the driving-comb electrode 1 141. To the driving-comb electrode 2 143, an anti-phase sinusoidal voltage 144 with the same offset is applied.

Please amend Page 20, lines 19 through page 21, line 2 as follows:

To sense the displacement induced by Coriolis force, the sensing electrodes 145, 146 are connected to the negative input of the two charge amplifiers 147, 148. The moving parts and the substrate are grounded. The tuning voltage V_T 149 is applied to the positive input terminals of the charge amplifiers 147, 148. This tuning voltage is used to control the resonant frequency of the sensing mode. In this setup, the dc voltage of V_T appears at the output of the charge amplifier. To remove the dc voltage, ~~a~~ high-pass filters 150, 151 are ~~is~~ used. The modulated output voltage is obtained by subtracting the two output signals of the high pass filters 150, 151. Finally, the angular rate is obtained by demodulating the output signal.

Please amend Page 21, lines 3 through 21 as follows:

The effect of the parasitic capacitances is analyzed . Fig. 15 shows possible configurations of parasitic capacitance and an equivalent circuit representation. In Fig. 15a, $C_{P,SS}$ is the capacitance between the two stationary sensing electrodes (155, 156). It is calculated to be 14.17 fF for the structural thickness of 40μm. The capacitance between the sensing electrode and the substrate $C_{P,S}$ (157) is calculated to be 41 pF for the insulating oxide thickness of 0.12μm. The capacitance between the movable structure (158) and the substrate $C_{P,M}$ (159) is calculated to be 107.5 pF for the insulting oxide thickness of 0.12μm. The values are calculated using the parallel-plate approximation. In the calculations, it is assumed that the surfaces of substrate facing the sensing electrodes or facing the electrodes connected to the movable structure are in an accumulation state. This assumption is very reasonable because the surface is highly doped with phosphorus and the operation voltage is in the range of several volts. In the equivalent circuit model, $C_{P,M}$ disappears

since the substrate and the movable structure are grounded together. The $C_{P,SS}$ also disappears since the two terminals of $C_{P,SS}$ are connected to the negative input terminals of the charge amplifiers, where constant voltage of V_T is maintained by the virtual ground effect. The $C_{P,S}$ can affect the output of the charge amplifiers. However, if the value of $C_{P,S}$ does not change, the effect is none. To keep $C_{P,S}$ constant, a highly doped silicon wafer is used and thus, the surface of the substrate is always in an accumulation state.